We claim:

1. An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data and context information; and

a co-processor comprising a plurality of state information buffers for storing state information associated with events wherein each of said state information buffers having an in-use counter indicating the number of events associated with the contents of said buffer.

2. The integrated circuit of claim 1 wherein said co-processor comprises a plurality of context buffers for storing context information associated with a plurality of events.

3. The integrated circuit of claim 2 wherein said co-processor comprises an in-use counter associated with each of said context buffers.

4. The integrated circuit of claim 1 wherein said co-processor comprises a plurality of data buffers for storing data.

5. The integrated circuit of claim 4 wherein said co-processor comprises an in-use counter associated with each of said data buffers.

6. The integrated circuit of claim 1 wherein said integrated circuit comprises a plurality of data buffers each having an in-use counter whereby data can be transferred from one event to another event by changing information in a data buffer.

7. The integrated circuit of claim 1 wherein said integrated circuit comprises a plurality of buffers for data associated with events and a plurality of buffers for context associated with events.

8. The integrated circuit of claim 7 wherein said integrated circuit comprises an in-use counter associated with each of said buffers.

9. The integrated circuit of claim 1 wherein said co-processor comprises a plurality of data only information buffers, a plurality of context information buffers, an in-use counter for each of said data only buffers and an in-use counter for each of said context buffers.

10. The integrated circuit of claim 9 where data can be passed from one event to another event by changing the data in one of said state information buffers.

11. A method of processing events related to communication packets in an integrated circuit which includes a core processor and a co-processor having a state information buffer for storing state information for an event separate from the data associated with said event, said state information buffer having an associated in use counter, the method comprising:

incrementing the in-use counter associated with said state information buffer when an event is associated with said state information buffer; and

decrementing the in-use counter of said state information buffer when said event associated with said buffer is finished.

12. The method of claim 11 wherein said integrated circuit comprises a plurality of state information buffers.

13. The method of claim 11 wherein said integrated circuit comprises a context buffer and an in-use counter for said context information buffer and the method further comprises:

incrementing the in-use counter associated with said context buffer when an event is associated with said context buffer; and

decrementing the in-use counter of said context buffer when said events associated with said context buffer is finished.

14. The method of claim 11 wherein said integrated circuit comprises a data only buffer to store data associated with an event.

15. The method of claim 11 wherein said integrated circuit comprises a data only buffer to store data associated with an event and an in-use counter associated with said data only buffer and the method further comprises:

incrementing the in-use counter associated with said data buffer when an event is associated with said data buffer; and

decrementing the in-use counter of said data buffer when said event associated with said data buffer is finished.

16. An integrated circuit for processing events associated with communication packets which includes a core processor and a co-processor, the improvement which comprises, separate buffers for data and state information and in-use counters for all of said buffers, whereby the contents of a data can be passed from one event to another event,

each of said events having state information in a separate state information buffer.

17. The integrated circuit of claim 16 which includes context information buffers.

18. The integrated circuit of claim 17 which includes in-use counters for said context information buffers.

19. The integrated circuit of claim 16 including a plurality of data buffers and a plurality of state information buffers.

20. The integrated circuit of claim 16 which includes a plurality of data buffers, a plurality of state information buffers and a plurality of context information buffers, each of said buffers having an in-use counter which is increments when an event is associated with the buffer and decremented when an event is finished utilizing the buffer.

21. An integrated circuit for processing events related to communication packets, said integrated circuit comprising:

a core processor configured to execute software to process a series of communication packets, the processing of each packet being an event and having associated data, state and context information; and

a co-processor having a plurality buffers which separately store data, state and context information associated with events wherein each of said data, state and context buffers having an in-use counter indicating the number of events associated with said buffer.